

### **Amendments to the Claims**

This listing of claims will replace all prior versions, and listings of claims in the application:

#### **Listing of Claims:**

Claim 1 (Original): A method of storing data comprising:

connecting a data line to a first sense amplifier when a first bit line is disconnected from the first sense amplifier;

connecting the first sense amplifier to the first bit line when the data line is disconnected from the first sense amplifier; and

connecting the data line to a second sense amplifier when the first bit line is connected to the first sense amplifier.

Claim 2 (Original): The method of claim 1, wherein connection between the data line and the first sense amplifier, and connection between the first bit line and the first sense amplifier, are controlled in response to a common signal.

Claim 3 (Original): The method of claim 1, further comprising connecting the second sense amplifier to a second bit line when the second sense amplifier is disconnected from the data line.

Claim 4 (Original): The method of claim 3, wherein the second bit line is included in a memory cell array block that is different from a memory cell array block in which the first bit line is included.

Claim 5 (Original): The method of claim 1, wherein the first bit line is connected to the first sense amplifier via a pair of transistors which are connected in parallel.

Claim 6 (Original): The method of claim 5, wherein the transistors include an N-channel transistor and a P-channel transistor, each of which is operated by complementary signals.

Claim 7 (Original): The method of claim 1, wherein the first bit line is connected to the first sense amplifier via a switching transistor, wherein the switching transistor is driven by a first voltage and then driven by a second voltage which is higher than the first voltage.

Claim 8 (Original): A method of storing data comprising:

transferring first data from a data line to a first sense amplifier when a first bit line is disconnected from the first sense amplifier;

transferring the first data from the first sense amplifier to the first bit line after the first sense amplifier is disconnected from the data line;

transferring second data from the data line to a second sense amplifier when the first bit line is connected to the first sense amplifier; and

transferring the second data from the second sense amplifier to a second bit line after the second sense amplifier is disconnected from the data line.

Claim 9 (Original): The method of claim 8, wherein the second bit line is included in a memory cell array block that is different from a memory cell array block in which the first bit line is included.

Claim 10 (Original): The method of claim 8, wherein the first data is transferred from the first sense amplifier to the first bit line via a pair of transistors which are connected in parallel.

Claim 11 (Original): The method of claim 10, wherein the transistors include an N-channel transistor and a P-channel transistor, each of which is operated by complementary signals.

Claim 12 (Original): The method of claim 8, wherein the first data is transferred from the first sense amplifier to the first bit line via a switching transistor, wherein the switching transistor is driven by a first voltage and then driven by a second voltage which is higher than the first voltage.

Claim 13 (Original): A method of storing data comprising:

transferring first data from a data line to a first sense amplifier, wherein the first data is latched in the first sense amplifier;

transferring the first data from the first sense amplifier to a first bit line; and

transferring second data from the data line to a second sense amplifier, wherein the second data is latched in the second sense amplifier,

wherein a period of latching the second data from the data line to the second sense amplifier, and a period of transferring the first data from the first sense amplifier to the first bit line, are overlapped.

Claim 14 (Original): The method of claim 13, wherein the second bit line is included in a memory cell array block that is different from a memory cell array block in which the first bit line is included.

Claim 15 (Original): The method of claim 13, wherein the first data is transferred from the first sense amplifier to the first bit line via a pair of transistors which are connected in parallel.

Claim 16 (Original): The method of claim 15, wherein the transistors include an N-channel transistor and a P-channel transistor, each of which is operated by complementary signals.

Claim 17 (Original): The method of claim 13, wherein the first data is transferred from the first sense amplifier to the first bit line via a switching transistor, wherein the switching transistor is driven by a first voltage and then driven by a second voltage which is higher than the first voltage.

Claim 18 (Original): A method of transferring data comprising:

supplying a first voltage to a switching transistor which is connected between a sense amplifier and a bit line, wherein data having a voltage drop caused by a threshold voltage of the switching transistor is transferred from the sense amplifier to the bit line by the switching transistor; and

supplying a second voltage which is higher than the first voltage to the switching transistor, wherein the data which does not have a voltage drop caused by the threshold voltage of the switching transistor is transferred from the sense amplifier to the bit line.

Claim 19 (Canceled)